

## CLAIMS:

1. A latch circuit (1) comprising,
  - a differential input with an inverting input (D+) and a non-inverting input (D-),
  - a differential output with an inverting output (Q+) and a non-inverting output (Q-),
- 5 - one of the outputs (Q-) being coupled to one of the inputs input (D+) having an opposite polarity,
- a control input for receiving a control signal ( $V_{CM}$ ) for determining a threshold for an input signal ( $In$ ) such that if the input signal is at larger than the threshold the non-inverting output s in a HIGH logic state and in a LOW state if the input signal is smaller than 10 the threshold, respectively.
2. A latch circuit as claimed in claim 1 comprising transistors, each transistor comprising a source, a gate and a drain, the latch further comprising,
  - a first pair of transistors comprising a first transistor (M1) and a second transistor (M3) having their sources coupled to each other,
  - a second pair of transistors comprising a third transistor (M4) and a fourth transistor (M5) having their sources coupled to each other,
  - a gate of the second transistor (M3) being coupled to a gate of the third transistor (M4) and further coupled to the control signal ( $V_{CM}$ ),
- 15 - a positive feedback from the non-inverting output (Q-) to a gate of the first transistor (M1),
- a pair of switches comprising a first switch (M2) and a second switch (M6) having their respective drains and sources coupled to the respective drains and sources of the first transistor (M1) and the fourth transistor (M5), respectively, and
- 20 - gate of the first switch (M2) being driven by the inverting clock signal ( $Ck+$ ) and gate of the second switch (M5) being driven by the non-inverting clock signal ( $Ck-$ ).
- 25 -
3. A latch as claimed in claim 2, wherein

- the sources of the first transistor (M1) and the second transistor (M3) are supplied by a first current source (I0),
- the sources of the third transistor (M4) and the fourth transistor (M5) are supplied by a second current source (I1).

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4. A latch circuit as claimed in claim 3, wherein the first current source (I0) and the second current source (I1) provide substantially equal currents.

5. A latch circuit as claimed in one of the claims 2 to 4, wherein the drain of  
10 the first transistor (M1) and the drain of the fourth transistor (M5) are coupled to each other and further coupled to a supply voltage (VDD) via a first resistor means (R1).

6. A latch circuit as claimed one of the claims 2 to 5, wherein the drain of the  
second transistor (M3) is coupled to a drain of the third transistor (M4), the drains being  
15 further coupled to the supply voltage (VDD) via a second resistor means (R2).

7. A latch circuit as claimed in one of the claims 2 to 7, wherein the second  
resistor means is coupled to a reference terminal (GND) via a third current source (I2).

20 8. A latch circuit as claimed in any of the preceding claims, wherein the first  
current source (I0) and the second current source (I1) comprises a series connection of a main  
current channel of a current source (M13, M14, M15, M16) and a third resistor means (R3).

9. A latch circuit as claimed in claim 8, wherein the controlled sources (M13,  
25 M14, M15, M16) are controlled by a voltage (VC).

10. A latch circuit as claimed in claim 1, adapted for differential input signals  
(In+, In-) and comprising a first latch portion (1') and second latch portion (1''), which are  
substantially identical, each latch portion comprising

30 - a differential input with an inverting input (D1+, D2+) and a non-inverting  
input (D1-, D2-),  
- a differential output with an inverting output (Q1+, Q2+) and a non-inverting  
output (Q1-, Q2-),

- one of the outputs (Q1-) of the first latch portion (1') being coupled to one of the inputs (D2+) having opposite polarity of the second latch portion (1''),
  - one of the outputs (Q2+) of the second latch portion being coupled to one of the inputs having opposite polarity of the first latch portion (D1-),
- 5 - a differential input signal (In+, In-) being provided at one of the inputs of the first latch portion (1') and to one of the inputs having an opposite polarity of the second latch portion (1''), respectively, and
  - each of the latch portions comprising a control input ( $V_{CM1}$ ,  $V_{CM2}$ ), which is coupled a respective control signal ( $V_{CM1}$ ,  $V_{CM2}$ ), which determines a threshold for the input
- 10 signal (In+, In-) such that if the input signal is at larger than the threshold the output latch is in a HIGH logic state and in a LOW state if the signal is smaller than the threshold, respectively.

11. A latch circuit as claimed in claim 10 comprising transistors, each transistor comprising a source, a gate and a drain, and wherein each latch portion (1'; 1'') comprises

- a first pair of transistors comprising a first transistor (M1A; M1B) and a second transistor (M3A; M3B), having their sources coupled each other, respectively
- a second pair of transistors comprising a third transistor (M4A; M4B) and a fourth transistor (M5A; M5B), having their sources coupled each other, respectively
- 20 - a gate of the second transistor (M3A; M3B) being coupled to a gate of the third transistor (M4A; M4B) respectively and further coupled to a DC voltage level ( $V_{CM}$ ),
- a pair of switches comprising a first switch (M2A; M2B) and a second switch (M6A; M6B), the switches including transistors having their respective drains and sources coupled to the respective drains and sources of the first transistor (M1A; M1B) and the fourth transistor (M5A; M5B), respectively,
- gate of the first switch (M2A; M2B) being driven by a binary clock signal ( $Ck^+$ ) and gate of the second switch (M6A; M6B) being driven by an inverted binary clock signal ( $Ck^-$ ), and
- the two latch portions (1', 1'') being crossed-coupled such that a gate of the first transistor (M1A; M1B) of a portion is coupled to the respective output of the other portion (INTQ-; INTQ+), respectively.

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12. A latch as claimed in Claim 11 wherein

- the sources of the first transistor (M1A, M1B) and the second transistor (M3A, M3B) are supplied by a first current source (I0),
- the sources of the third transistor (M4A, M4B) and the fourth transistor (M5A, M5B) are supplied by a second current source (I1).

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13. A latch circuit as claimed in claim 12, wherein the first current source (I0) and the second current source (I1) provide substantially equal currents.

14. A latch circuit as claimed in one of the claims 10 to 13, wherein the drain of  
10 the first transistor (M1A; M1B) and the drain of the fourth transistor (M5A; M5B) are coupled to each other respectively and further coupled to a supply voltage (VDD) via a first resistor means (R1).

15. A latch circuit as claimed in one of the claims 10 to 14, wherein the drain of  
15 the second transistor (M3A; M3B) is coupled to a drain of the third transistor (M4A; M4B), respectively the drains being further coupled to the supply voltage (VDD) via a second resistor means (R2).

16. A latch circuit as claimed in one of the claims 10 – 15, wherein the first  
20 current source (I0) and the second current source (I1) comprises a series connection of a main current channel of a controlled current source (M13, M14, M15, M16) and a third resistor means (R3).

17. A latch circuit as claimed in claim 16, wherein the controlled sources (M13,  
25 M14, M15, M16) are controlled by a voltage (VC).